14. (Amended) The semiconductor integrated circuit device according to claim 9, wherein the first wiring and the second wiring are arranged in an uppermost layer of the chip.

REMARKS

By this Second Preliminary Amendment, Applicants amend claims 1 and 9-14. Claims 1 and 4-14 remain pending. This Second Preliminary Amendment is in addition to the Preliminary Amendment filed on February 25, 2002.

In an Office Action dated October 24, 2001 for application no. 09/527,563, now abandoned, upon which this continuation application relies for priority, the Examiner objected to the specification under 35 U.S.C. § 132; rejected claims 1 and 4-14 under 35 U.S.C. § 112, first paragraph; and rejected claims 1 and 4-14 under 35 U.S.C. § 103(a) as unpatentable over so-called admitted prior art in view of U.S. Patent No. 5,031,072 to Malhi et al. ("Malhi").

In response to the Office Action, Applicants filed a Request for Reconsideration on January 18, 2002 and received an Advisory Action in which the Examiner stating that the Request for Reconsideration did not place the application in condition for allowance because "the specification does not disclose the limitations introduced in the amendment filed 8/8/01." The Examiner stated that paragraph at page 9, lines 8-15 of the specification of the present application "does not revel any isolation, but only that no via is present." And that the subject matter in the claims "must be described in the specification and not only shown in the drawings."

Written Description Requirement

Applicants respectfully traverse the § 132 objection and the § 112, first paragraph rejection. M.P.E.P. §2163.02 states the following:

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> [T]he fundamental factual inquiry [for determining compliance with the written description requirement] is whether the specification conveys with reasonable clarity to those skilled in the art that, as of the filing date sought, applicant was in possession of the invention as now claimed. See, e.g., *Vas-Cath*, Inc. v. Mahurkar, 935 F. 2d 1555, 1563-64... Possession may be shown in a variety of ways including ... the disclosure of *drawings* or structural chemical formulas that show that the invention was complete (emphasis added)...
>
> The subject matter of the claim need not be described literally (i.e., using the same terms or *in haec verba*) in order for the disclosure to satisfy the description requirement.

In *Vas-Cath*, the CAFC held that drawings alone could provide the "written description" required by § 112. *Id.* at 1564. In this application, the Applicants provide support for the claims in both the specification and drawings, even though the drawings alone could provide the written description requirement. Specifically, as pointed out in the amendment filed on February 25, 2002 in Application No. 09/527,563, the specification and the drawings of the present application support: 1) a third wiring being isolated from the second wiring, 2) a fourth wiring being isolated from the first wiring, and 3) a fourth wiring being shorter than the third wiring, as described below.

A third wiring being isolated from the second wiring

Fig. 2 shows a five-layered metal wiring, wherein a third wiring 24 is isolated from a second wiring 17. The specification describes this isolation when it states at page 9, lines 8-15:

> A via for connecting the third layer metal to the fourth layer metal positioned between the vias 15 and 34 is not formed. A via for connecting the second layer metal to the third layer metal between vias 18 and 25 is not formed, either. Likewise, a via for connecting the third layer metal to the fourth layer metal positioned between the vias 18 and 25 is not formed.

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Although the specification does not use the same terms as the claims, the disclosure provided in the specification and drawings describes a structure having a third wiring isolated from the second wiring, thereby satisfying the written description requirement.

Fourth wiring being isolated from the first wiring

Fig. 2 also shows a fourth wiring 33 being isolated from the first wiring 14. This isolation is also described in the specification at page 9, lines 8-15 (see above.)

Fourth wiring being shorter than the third wiring

Fig. 2 shows a fourth wiring 33 being shorter than a third wiring 24. Further, the specification describes this structure throughout the application. For example, at page 2, lines 18-26 of the present application a problem in the prior art is disclosed wherein a "wiring 17 between the pad 12b and the via 18 is rendered long, though the wiring 14 between the pad 12a and the via 15 is short" causes a "delay of the signal transmission." The specification for the present application further discloses at page 9, lines 22-27 that "the wiring length of the I/O slot can be shortened by the rewiring 24, 33 on the outermost periphery of the chip, and the delay in the signal transmission can be improved."

Although the specification does not use the same terms as the claims, the disclosure provided in the specification and drawings describes a structure having a fourth wiring shorter than the third wiring, thereby satisfying the written description requirement.

Accordingly, because the amendment filed in application no. 09/527,563 on August 8, 2001 did not, in fact, introduce any new matter, Applicants respectfully

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request that the objection under 35 U.S.C. § 132 and the rejection under 35 U.S.C. first paragraph be withdrawn, in so far as they are applied to the pending claims of the present application.

In making the various references to the specification and drawings set forth above, it is to be understood that Applicants are in no way intending to limit the scope of the claims to the exemplary embodiments shown in the drawings and described in the specification. Rather, Applicants expressly affirm that they are entitled to have the claims interpreted broadly, to the maximum extent permitted by statute, regulation and applicable case law.

Rejection under 35 U.S.C. § 103(a)

In so far as the Examiner may apply a combination of Applicants' so-called admitted prior art (Fig. 4) and Malhi to claims 1 and 9 of the present application, Applicants distinguish the claimed structure from the combination of Malhi and Fig. 4 of the present application.

First, Fig. 4 of the present application does not disclose or suggest at least a third or fourth wiring, as claimed.

Second, Malhi shows in Fig. 17 a solder pad 146 and a connector pad 148 arranged on a baseboard 120. Chips are connected to each other via conductor lines 140 and pads 146, 148, all of which are located on the surface of baseboard 120. Thus, Malhi does not teach or suggest at least "first and second I/O slots are arranged on the same wiring level" and first and second pads "arranged on a wiring layer different from the first I/O slot," as recited in independent claims 1 and 9, let alone a "third wiring arranged in an outermost peripheral portion of the chip and serving to connect the first

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wiring to the second I/O slot" nor a "fourth wiring arranged in the outermost peripheral region of the chip and serving to connect the other end of the second wiring to the first I/O slot." Accordingly, claims 1 and 9 are patentable under 35 U.S.C. § 103(a) over Applicants' so-called admitted prior art and Malhi whether taken alone or together. Claims 4-8 and 10-14 are patentable as well, at least in view of their dependence from claims 1 and 9, respectively.

Additionally, Malhi describes a structure wherein the conductor line of the baseboard is individually designed according to each product design. In contrast, according to the present invention a fixed, standard pattern is used among various product designs. Thus, the Malhi structure is fundamentally different from the structure claimed in the present invention and the structure disclosed in Applicants' so-called admitted prior art, and there is no motivation for combining the Malhi structure with the structure shown in Fig. 4 of the present application.

CONCLUSION

Attached hereto is a marked-up version of the changes made to the claims by this amendment. The attachment is captioned "**Appendix to the Preliminary Amendment of April 24, 2002**" Deletions appear as normal text surrounded by [ ] and additions appear as underlined text.

If there is any fee due in connection with the filing of this Preliminary Amendment, please charge the fee to our Deposit Account No. 06-0916.

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Respectfully submitted,

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Dated: April 24, 2002

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APPENDIX TO AMENDMENT OF APRIL 24, 2002

Version with Markings to Show Changes Made

Amendments to the Claims

Please amend claims 1 and 9-14, as follows:

1. (Twice Amended) A semiconductor integrated circuit device, comprising:

first and second I/O slots arranged on the same wiring layer in parallel along a peripheral portion of a chip within an inner region of the chip and connected to input/output cells of the chip;

a first pad arranged [above said first I/O slot] on a wiring layer different from said first I/O slot;

a second pad arranged on a wiring layer different from [above] the first I/O slot and comprising a predetermined distance apart from the first pad in a direction extending from the peripheral portion of the chip toward the central portion;

a first wiring [having] comprising one end positioned in said first pad and [having] comprising the other end positioned in the peripheral portion of the inner region of the chip above the first I/O slot;

a second wiring [having] comprising one end positioned in the second pad and [having] comprising the other end positioned in the peripheral portion of the inner region of the chip above the second I/O slot;

a third wiring arranged in an outermost peripheral portion of the chip and serving to connect the other end of the first wiring to the second I/O slot; and

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a fourth wiring arranged in the outermost peripheral region of the chip and serving to connect the other end of the second wiring to the first I/O slot[, the fourth wiring being isolated from the first wiring].

9. (Amended) A semiconductor integrated circuit device, comprising

first and second I/O slots arranged on the same wiring layer in parallel along a peripheral portion of a chip within an inner region of the chip and connected to input/output cells of the chip,

a first pad arranged [above] on a wiring layer different from the first I/O slot;

a second pad arranged [above] on a wiring layer different from the first I/O slot and comprising a predetermined distance apart from the first pad in a direction extending from the peripheral portion of the chip toward the central portion;

a first wiring [having] comprising one end positioned in the first pad and [having] comprising the other end positioned in the peripheral portion of the inner region of the chip above the first I/O slot;

a second wiring [having] comprising one end positioned in said second pad and [having] comprising the other end positioned in the peripheral portion of the inner region of the chip above the second I/O slot;

a third wiring arranged in an outermost peripheral region of the chip and serving to connect the other end of the first wiring to the second I/O slot, and

a fourth wiring arranged in the outermost peripheral region of the chip and serving to connect the other end of the second wiring to the first I/O slot, the fourth wiring being shorter than the third wiring.

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10. (Amended) The semiconductor integrated circuit device according to claim [7] 9, wherein the third wiring is isolated from the second wiring, and the fourth wiring is isolated from the first wiring.

11. (Amended) The semiconductor integrated circuit device according to claim [7] 9, wherein the third wiring and the fourth wiring do not overlap.

12. (Amended) The semiconductor integrated circuit device according to claim [7] 9, wherein the first and second I/O slots, the first and second pads and the first and second wiring are each designed and fixed in advance.

13. (Amended) The semiconductor integrated circuit device according to claim [7] 9, wherein the first wiring and the second wiring are the same in wiring level.

14. (Amended) The semiconductor integrated circuit device according to claim [7] 9, wherein the first wiring and the second wiring are arranged in an uppermost layer of the chip.

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